622 can be formed above pre-HVNWs **610**, **611**, and **612**, respectively. After forming pre-HVNWs **610**, **611**, and **612** and PBLs **620**, **621**, and **622**, a P-type epitaxial layer can be formed on P-sub **100**.

[0039] In some embodiments, multiple N-type buried layers (NBLs) and multiple PBLs can be included in a device. The multiple NBLs and PBLs can be alternatively arranged. FIG. **7** schematically illustrates a cross-sectional view of a device **70** according to such an embodiment. Device **70** has a structure similar to that of device **10**, except that three (3) PBLs **710**, **711**, and **712**, and two (2) NBLs **720** and **721** are formed between HVNW **120** and P-sub **100**. PBLs **710**, **711**, and **712**, and NBLs **720** and **721** are alternately arranged. Specifically, PBLs **710**, **711**, and **712** are spaced apart from each other, and each one of NBLs **720** and **721** is arranged between two adjacent PBLs. That is, NBL **720** is arranged between PBLs **710** and **711**, and NBL **721** is arranged between PBLs **711** and **712**. The widths of PBLs **710**, **711**, and **712**, and NBLs **720** and **721** can be varied in view of various design considerations. In addition, the numbers of PBLs and NBLs can be varied. During a fabrication process of device **70**, PBLs **710**, **711**, and **712** can be formed in P-sub **100**, and then NBLs **720** and **721** can be formed between PBLs **710**, **711**, and **712**. After forming PBLs **710**, **711**, and **712**, and NBLs **720** and **721**, a P-type epitaxial layer can be formed on P-sub **100**.

[0040] While the embodiment described above is directed to N-type LDMOS device **10** shown in FIG. **1** and fabrication methods thereof shown in FIGS. **2A-2N**, those skilled in the art will now appreciate that the disclosed concepts are equally applicable to a P-type LDMOS device. Those skilled in the art will also appreciate that the disclosed concepts are applicable to other semiconductor devices and the fabrication methods thereof, such as insulated-gate bipolar transistor (IGBT) devices and diodes.

[0041] FIG. **8** schematically Illustrates a cross-sectional view of an insulated gate bipolar transistor (IGBT) **80**, according to an illustrated embodiment. IGBT **80** has a structure similar to that of device **10**, except that first N^+-region **175** is replaced with a P^+-region **875** which functions as a drain region.

[0042] FIG. **9** schematically illustrates a cross-sectional view of an ultra-HV diode **90**, according to an illustrated embodiment. Diode **90** has a structure similar to that of device **10**, except that a contact layer **900** includes a contact portion **910** that conductively contacts second N^+-region **176**, first P^+-region **180**, and second P^+-region **181**.

[0043] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

1. A semiconductor device, comprising:
- a substrate having a first conductivity type;
- a high-voltage well having a second conductivity type and formed in the substrate;
- a drift region formed in the high-voltage well; and
- a buried layer having the first conductivity type formed below the high-voltage well and vertically aligned with the drift region,
- wherein the drift region includes:
  - a top region having the first conductivity type and formed in the high-voltage well; and
  - a grade region having the second conductivity type and formed above the too region.

2. The semiconductor device of claim **1**, further including a pre-high-voltage well having the second conductivity type and formed below the buried layer.

3. The semiconductor device of claim **1**, wherein the buried layer includes a plurality of buried layers having the first conductivity type formed below the high-voltage well and vertically aligned with the drift region, the plurality of buried layers being spaced apart from each other,
- the device further comprising a plurality of pre-high-voltage wells having the second conductivity type, each pre-high-voltage well being formed below a respective one of the buried layers.

4. The semiconductor device of claim **1**, wherein the buried layer includes a plurality of first buried layers having the first conductivity type formed below the high-voltage well and vertically aligned with the drift region, the plurality of first buried layers being spaced apart from each other,
- the device further comprising a plurality of second buried layers having the second conductivity type formed below the high-voltage well, each one of the plurality of second buried layers being formed between two adjacent first buried layers.

5. (canceled)

6. The semiconductor device of claim **1**, wherein the semiconductor device is a lateral diffused metal oxide semiconductor (LDMOS) device,
- the semiconductor device further including a drain region having the second conductivity type formed in the high-voltage well.

7. The semiconductor device of claim **1**, wherein the semiconductor device is an insulated gate bipolar transistor,
- the semiconductor device further including a drain region having the first conductivity type formed in the high-voltage well.

8. The semiconductor device of claim **1**, wherein the semiconductor device is a diode.

9. The semiconductor device of claim **1**, wherein the first conductivity type is P-type and the second conductivity type is N-type.

10. The semiconductor device of claim **1**, wherein the first conductivity type is N-type and the second conductivity type is P-type.

11. The semiconductor device of claim **1**, further including:
- a source well having the first conductivity type and formed in the high-voltage well, the source well being spaced apart from the drift region;
- a source region formed in the source well;
- a drain region formed in the high-voltage well and spaced apart from the drift region;
- a gate oxide layer disposed on the substrate between the source region and the drain region; and
- a gate layer disposed on the gate oxide layer.

12. The semiconductor device of claim **1**, further including:
- an interlayer dielectric layer disposed on the substrate; and
- a contact layer disposed on the interlayer dielectric layer.

13. A method for fabricating a semiconductor device, the method comprising:
- providing a substrate having a first conductivity type;
- forming a buried layer having the first conductivity type in the substrate;